FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

ATTY DKT NO.	SERIAL NO.
2867-127	09/879,806
APPLICANT: Alexander W. Hietala	
FILING DATE: 6/12/2001	GROUP: TBA

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CL.	SUBCL.	FILING DATE IF APPROP.
JP	A	4,965,474	10/1990	Childers et al.	307	542	
JP	B	5,341,033	08/1994	Koker	307	290	
JP	C	5,563,532	10/1996	Wu et al.	327	34	
JP	D	6,275,083	08/2001	Martinez et al.	327	218	
JP	E	6,323,709	11/2001	Kulkarni et al.	327	195	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CL.	SUBCL	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent pages, etc.)

EXAMINER: JP

DATE CONSIDERED: 8/5/05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	APPLICANT Hietala	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE 06/12/2001	GROUP 2631

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CL.	SUBCL.	FILING DATE IF APPROP.
JP	A	4,609,881	09/1986	Wells	331	1 A	
JP	B	4,920,282	04/1990	Muraoka	307	442	
JP	C	4,953,187	08/1990	Herold	337	48	
JP	D	4,965,531	10/1990	Riley	331	1 A	
JP	E	4,991,187	02/1991	Herold	337	48	
JP	F	5,022,054	06/1991	Wang	375	64	
JP	G	5,038,117	08/1991	Miller	331	16	
JP	H	5,055,800	10/1991	Black	331	1 A	
JP	I	5,055,802	10/1991	Hietala	331	16	
JP	J	5,058,427	10/1991	Brandt	73	384	

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		DOCUMENT NO.	DATE	COUNTRY	CL.	SUBCL	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent pages, etc.)

JP	K	Chang, Byngsoo, et al. "A 1.2 GHz CMOS Dual-Modulus Prescaler Using New Dynamic D-Type Flip-Flops," IEEE Journal of Solid-State Circuits, Vol. 31, No. 5, May, 1996, pages 749-752.
JP	L	Huang, Qiuting, and Rogenmoser, Robert, "Speed Optimization of Edge-Triggered CMOS Circuits for Gigahertz Single-Phase Clocks," IEEE Journal of Solid-State Circuits, Vol. 31, No. 3, March, 1996, pages 456-465.
JP	M	Motorola Semiconductor Technical Data, "The Technique of Direct Programming by Using a Two-Modulus Prescaler," Originally printed May 1981, reformatted October 1995, Document no. AN827/D.

EXAMINER	DATE CONSIDERED
	8/8/05

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EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CL.	SUBCL.	FILING DATE IF APPROP.
	N	5,068,875	11/1991	Quintin	375	78	
	O	5,070,310	12/1991	Hietala	331	1 A	
	P	5,079,522	01/1992	Owen	331	16	
	Q	5,093,632	03/1992	Hietala	331	1 A	
	R	5,111,162	05/1992	Hietala	332	127	
	S	5,166,642	11/1992	Hietala	331	1 A	
	T	5,281,865	01/1994	Yamashita	307	279	
	U	5,301,367	04/1994	Heinonen	455	76	
	V	5,337,024	08/1994	Collins	332	127	
	W	5,365,548	11/1994	Baker	375	62	
	X	5,493,700	02/1996	Hietala	455	75	
	Y	5,495,206	02/1996	Hietala	331	1 A	

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		DOCUMENT NO.	DATE	COUNTRY	CL.	SUBCL	TRANSLATION	
							YES	NO

OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent pages, etc.)

	Z	Owen, David, "Fractional-N Synthesizers," IFR Application Note, IFR Americas, 2001, www.ifrsys.com
	AA	Pohjonen, H. and Ronkainen, H., "A 1 GHz CMOS Prescaler for RF Synthesizers," 1988 Proceedings of ISCAS, pages 377-380, CH2458-8/88/0000-0377.
	BB	Rogenmoser, R. et al., "1.57 GHz Asynchronous and 1.4 GHz Dual-Modulus 1.2 micrometer CMOS Prescalers," IEEE Customer Integrated Circuits Conference, 1994, pages 387-390, 0-7803-1886-2/94.

EXAMINER	DATE CONSIDERED
	12/05

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EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CL.	SUBCL.	FILING DATE IF APPROP.
JP	CC	5,552,738	09/1996	Ko	327	203	
JP	DD	5,592,114	01/1997	Wu	327	208	
JP	EE	5,684,795	11/1997	Daniel	370	347	
JP	FF	5,745,848	04/1998	Robin	455	296	
JP	GG	5,777,521	07/1998	Gillig	331	16	
JP	HH	5,778,028	07/1998	Turner	375	229	
JP	II	5,822,366	10/1998	Rapeli	375	219	
JP	JJ	5,825,257	10/1998	Klymyshyn	332	100	
JP	KK	5,857,004	01/1999	Abe	375	344	
JP	LL	5,859,890	01/1999	Shurboff	377	48	
JP	MM	5,883,930	03/1999	Fukushi	375	376	
JP	NN	5,892,385	04/1999	Hashiguchi	327	333	

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							YES	NO

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JP	OO	Yang, Ching-Yuan, and Liu, Shen-Iuan, "Fast-Switching Frequency Synthesizer with a Discriminator-Aided Phase Detector," IEEE Journal of Solid-State Circuits, Vol. 35, No. 10, October 2000, pages 1445-1452, 0018-9200/00.
JP	PP	Yuan, Jiren, and Svensson, Christer, "High-Speed CMOS Circuit Technique," IEEE Journal of Solid-State Circuits, Vol. 24, No. 1, February 1989, pages 62-70, 0018-9200/89.
JP	QQ	Yuan, Jiren and Svensson, Christer, "New Single-Clock CMOS Latches and Flipflops with Improved Speed and Power Savings," IEEE Journal of Solid-State Circuits, Vol. 32, No. 1, January 1997, pages 62-69, 0018-9200/97.

EXAMINER	DATE CONSIDERED
JM	8/8/05

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EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CL.	SUBCL.	FILING DATE IF APPROP.
JP	RR	5,898,330	04/1999	Klass	327	210	
JP	SS	5,900,758	05/1999	Kanno	327	201	
JP	TT	5,917,355	06/1999	Klass	327	208	
JP	UU	5,920,556	07/1999	Jorgensen	370	350	
JP	VV	5,933,038	08/1999	Klass	327	208	
JP	WW	5,943,613	08/1999	Wendelrup	455	343	
JP	XX	6,008,703	12/1999	Perrott	332	100	
JP	YY	6,008,704	12/1999	Opsahl	332	127	
JP	ZZ	6,043,696	03/2000	Klass	327	211	
JP	AAA	6,060,927	05/2000	Lee	327	218	
JP	BBB	6,064,272	05/2000	Rhee	331	16	
JP	CCC	6,097,259	08/2000	Saito	332	103	

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							YES	NO

OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent pages, etc.)

JP	DDD	Razavi, Behzad, "RF Microelectronics," Prentice Hall PTR, Upper Saddle River, NJ, 1998.

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JP	EEE	6,100,730	08/2000	Davis	327	117	
JP	FFF	6,121,807	09/2000	Klass	327	218	
JP	GGG	6,154,077	11/2000	Waible	327	185	
JP	HHH	6,163,710	12/2000	Blaser	455	552	

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